AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A data processor comprising:

a receiving unit for receiving a series of data including a predetermined ~~marks~~ mark for detecting synchronization and generating ~~a plurality of~~ parallel data from the series of data; and

a plurality of detecting units being provided at each bit position of the parallel data and for detecting said predetermined ~~marks~~ mark for detecting synchronization from the ~~plurality of~~ parallel data.

2. (Previously Presented) A data processor according to claim 1, wherein said plurality of detecting units detect the predetermined marks for detecting synchronization in a predetermined bit width among the series of data in parallel condition.

3. (Previously Presented) A data processor according to claim 1, further comprising a generation timing selecting unit for selecting generation timing of a window for detecting the predetermined marks based on the predetermined marks for detecting synchronization.

4. (Previously Presented) A data processor according to claim 1, further comprising a data demodulating unit for demodulating the series of data between the predetermined marks for detecting synchronization based on the predetermined marks for detecting synchronization.

5. (Previously Presented) A data processor according to claim 1, further comprising a detection line memory unit for storing a detection line based on the predetermined marks for detecting synchronization.

6. (Previously Presented) A data processor according to claim 1, further comprising a data selecting unit for selecting data based on the predetermined marks for detecting synchronization.

7. (Previously Presented) A data processor according to claim 1, further comprising a data counting unit for counting the series of data between the predetermined marks for detecting synchronization based on the predetermined marks for detecting synchronization.

8. (Canceled).

9. (Previously Presented) A data processor according to claim 1, wherein said receiving unit is provided with a shift register to input the plurality of parallel data connected with the detecting units in the same number as the number of parallel data.

10. (Currently Amended) A data processor for detecting a predetermined ~~marks~~ mark for detecting synchronization included in a series of data read from a memory medium in order to establish synchronization at a time of transferring the series of data to a controller unit from a read channel unit, comprising:

a receiving unit for receiving the series of data including the predetermined ~~marks~~ mark for detecting synchronization and generating ~~a plurality of~~ parallel data from the series of data; and

a plurality of detecting units being provided at each bit position of the parallel data and for detecting said predetermined ~~marks~~ mark for detecting synchronization from the ~~plurality of~~ parallel data.

11. (Previously Presented) A data processing method comprising the following steps of:

receiving a series of data including predetermined marks for detecting synchronization;

generating a plurality of parallel data from the series of data;

detecting the predetermined marks for detecting synchronization from said plurality of parallel data to establish synchronization of the series of data; and

demodulating the series of data based on the predetermined marks for detecting synchronization included in the series of data.

12. (Previously Presented) A data processing method according to claim 11, wherein the predetermined marks for detecting synchronization are detected in predetermined bit widths of the series of data in parallel condition.

13. (Previously Presented) A data processing method according to claim 11, wherein generation timing of a window for detecting predetermined marks is selected based on the detected predetermined marks for detecting synchronization.

14. (Previously Presented) A data processing method according to claim 11, wherein a detection line is stored based on the detected predetermined marks for detecting synchronization.

15. (Previously Presented) A data processing method according to claim 11, wherein data is selected based on the detected predetermined marks for detecting synchronization.

16. (Original) A data processing method according to claim 11, wherein data between the detected predetermined marks for detecting synchronization is counted up.

17. (Currently Amended) A data processor according to claim 1, wherein said plurality of detecting units detect the corresponding each of ~~the~~ a plurality of parallel data.